UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/032,863	03/02/1998	GORDON F. GRIGOR	0100.01117	1397

23418 7590 10/01/2003

VEDDER PRICE KAUFMAN & KAMMHOLZ
222 N. LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
NGUYEN, KEVIN M	

ART UNIT	PAPER NUMBER
2674	32

DATE MAILED: 10/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/032,863	GRIGOR ET AL.	
	Examiner	Art Unit	
	Kevin M. Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24,29-33,38-53 and 56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24,29-33,38-53 and 56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The amendment filed on 7/24/2003 is entered. However, the rejection of claims 24, 29-33, 38-53 and 56 are maintained.

2. The indicated allowability of claim 54 is withdrawn in view of the previously cited reference(s) to Zenda (US 4,980,678). Rejections based on the previously cited reference(s) follow.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 24, 29, 31-33, 38, 40-46, 48-52 and 56 are rejected under 35 U.S.C. 102(b) as being anticipated by Zenda (US 4,980,678) hereinafter Zenda '678.

5. *As to claims 24, and 33*, Zenda '678 teaches a video graphics processing circuit associated with a digital storage medium for storing programming instruction, comprising a central processing unit (CPU) (1); and

a main memory 17 and V-RAM 15 operably coupled to the CPU (1), wherein the main memory 17 and V-RAM 15 store programming instructions that, when executed by a CPU 1, cause a D-flip flop 59 that controls gate 55 and 57 (switches 55 and 57) of the CPU 1 to

(a) receive display preferences regarding two display CRT 19 and PDP 21 (see figure 8, column 6, lines 16-53);

(b) determine whether the display preferences can be fulfilled in observance of at least one of: configuration properties of the two displays (CRT 19 and PDP 21) and configuration properties of a computing system, the D-flip flop 59 that controls gate 55 and 57 (switches 55 and 57) for determining whether a current configuration of two displays CRT 19 and PDP 21 to the computing system can be reconfigured such that the display preferences can be fulfilled while maintaining effective configuration of the current configuration when the display preferences cannot be fulfilled;

(c) configure the computing system and two displays CRT 19 and PDP 21 in accordance with the display preferences when the display preferences can be fulfilled, and reconfigure operable coupling of the multiple displays to the computing system such that two displays CRT 19 and PDP 21 are configured in accordance with the display preferences when the current configuration can be reconfigured (see figure 11A and 11B, column 6, line 61 through column 7, 8, line 14);

(d) operably couple a display controller 25 of a computing system to two displays (CRT 19 and PDP 21), the display controller 25 providing display data to two displays (CRT 19 and PDP 21);

(e) operably couple the CRT controller (25) to a plurality of bit maps V-RAM 15, each of the plurality of bit maps V-RAM 15 and the CRT controller 25 storing separate display data and the CRT control 25 retrieving the display data from the plurality of bit maps V-RAM 15; and

(f) operably couple the CRT/PDP controller (25) to a plurality of display driver CRT (19) and PDP (21) such that a first display driver CRT (19) is coupled to a first

screen memory portion (5) and a second memory portion "V-RAM (15)", each of display driver CRT (19) and PDP (21) writing the separate display data to the plurality of bit maps V-RAM 15 (see figure 8, column 6, lines 16-53).

As to claims 29, 38, Zenda '678 teaches the video graphics processing circuit associated with a digital storage medium, the main memory 17, and V-RAM 15 for storing programming instruction that cause the CPU 1 to operable couple a first display controller 12 coupling a first display CRT 19 and a second display controller 14 coupling a second PDP 19 (see figure 8, column 6, lines 16-53).

As to claims 31, 32, 40, 41, Zenda '678 teaches the video graphics processing circuit associated with a digital storage medium, the main memory 17, and V-RAM 15 for storing programming instruction that cause the CPU 1 to operable couple at least two display controller 12 and 14 coupling to one screen memory (V-RAM 15) (see figure 8, column 6, lines 16-53).

6. *As to claim 42*, Zenda '678 teaches a video graphics processing circuit for displaying at least one image on two displays CRT 19 and PDP 31, comprising:

two display CRT controller 12 and PDP 14 included on a single video graphics card (see figure 8);

two CRT driver 19 and PDP driver 21;

maim memory 17 and V-RAM 15, wherein at least a bit maps of V-RAM 15 is screen memory, the V-RAM having a plurality of bit maps, each of bit map storing separate display data (see figure 10, column 7, lines 13-41);

coupling module (gate 55 and gate 57) coupled to two display CRT 19 and PDP 21 and the V-RAM 15;

coupling controller "D-flip flop 59 controls switches 55 and 57" operably coupled to receive display preferences and to determine whether the display preferences can be fulfilled in observance of configuration properties, the display preferences including at least one of displaying image on more than one of displays, displays separate images on each of the displays, displaying a portion of the image one of the displays and displaying the image on another one of two display CRT 19 and PDP 21, providing different refresh rates for at least two of the displays, providing different resolutions for at least two of displays, selecting one of the displays to display a predetermined type of image, and displaying a first portion of the image on a first one of the displays and displaying a second portion of the image on a second one of the displays;

wherein, when the display preferences can be fulfilled, the D-flip flop 59 provides configuration requirements to the gates 55 and 57, the gates 55 and 57, based on the configuration requirements, operably couples at least one of the two display controller CRT 12 and PDP 14 with at least a portion of the V-RAM 15, such that a first display driver CRT (19) is coupled to a first screen memory portion (5) and a second memory portion "V-RAM (15)", and with at least one display, a respective display driver of the two display driver CRT 19 and PDP 21 thereby writing respective separate display data to a respective one of the plurality of bit maps V-RAM 15, and wherein the at least one of two display controller CRT 12 and PDP 14 retrieves display data from the at least one bit map of V-RAM 15 and provides the display data to the at least one display, and

wherein the D-flip flop 59 that controls the switches 55 and 57 when the display preferences cannot be fulfilled but a current configuration of two display controllers CRT 12 and PDP 14 to the at least one display can be reconfigured such that the display preferences can be fulfilled while maintaining effective configuration of the current configuration (see figure 8, 11A and 11B, column 6, line 16 through column 7, 8, line 14).

As to claim 43, Zenda '678 teaches a graphics engine (PD setting control circuit 29 and CRT controller 25) coupling to at least one CRT controller 12 and at least one of the CRT driver 19 (figure 8).

As to claim 44, Zenda '678 teaches a keyboard 16 (user interface, figure 8).

As to claim 45, Zenda '678 teaches BIOS ROM 17, set-up RAM 24 comprising properties memory (CRT pallet data buffer 5 and PDP pallet data buffer 7) that stores configuration properties of two CRT and PDP controllers 12 and 14 and the at least one CRT display 19, wherein the configuration properties include at least one of: limitations of two CRT and PDP controllers 12 and 14 and the at least one CRT display 19 and operational rules of the two CRT and PDP controller 12 and 14 and the at least one CRT display 19 (figure 8, column 6, lines 16-53).

As to claim 46, Zenda '678 teaches a video graphics processing circuit having first display controller 12 coupling to a first display CRT 19, a second display controller 14 coupling to a second display PDP 21 (figure 8, column 6, lines 16-53).

As to claim 48, Zenda '678 teaches a video graphics processing circuit having a first controller 12 and a second controller 14 to one V-RAM 15 (figure 8, column 6, lines 16-53).

7. *As to claim 49*, Zenda '678 teaches a video graphics processing apparatus having V-RAM 15, two CRT controller 12 and PDP controller 14, two display CRT driver 19 and PDP driver 21, a gate 55 and a gate 57 (coupling module), D-flip flop 59 (coupling controller), wherein the configuration properties comprise means for causing the coupling controller 59 to couple a first display driver 19 of the plurality of display drivers (19, 21) to a first (5) and a second screen memory portion (15) of the plurality of screen memory portions (5, 7, 15) (see figure 8, column 6, lines 16-53).

As to claim 50, Zenda '678 teaches a graphics engine (PD setting control circuit 29, and CRT controller 25) coupling to plurality of V-RAM 15 (figure 8, column 6, lines 16-53).

As to claim 51, Zenda 678 teaches a user interface 16 (see figure 8).

As to claim 52, Zenda '678 teaches a V-RAM 15 having display refresh rate, display resolution, and type of display (figure 8, column 6, lines 16-53).

As to claim 53, Zenda '678 teaches the coupling controller (59) to couple a first display controller (12) of the plurality of display controllers (12, 14) to a first and a second display of the plurality of displays (19, 21) (see figure 8, column 6, lines 16-53).

As to claim 56, Zenda '678 teaches a controller 25 which couples a V-RAM 15 to more than one of the plurality of display controllers (12, 14) (see figure 8, column 6, lines 16-53).

8. Claims 30, 39 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zenda '678 in view of Zenda (US 5,559,525) hereinafter Zenda '525.

As to claims 30, 39 and 47, Zenda '678 teaches all of the claimed limitations of claims 24, 33, 42, except for "the first display controller couples to a third display." However, Zenda '525 teaches a related video graphics processing circuit associated with a digital storage medium comprising a first display controller (87) coupling a third color CRT (107) (see figure 3A, column 9, lines 8-17). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the first display controller (87) coupling the third CRT (107) taught by Zenda '525 for Zenda '678's video graphics processing system because this would provide the additional graphics subsystem can be attached and being capable of displaying image data from a built-in graphics subsystem and the optional graphics subsystem on an flat panel display unit (column 2, lines 52-55 of Zenda '525).

Response to Arguments

9. Applicant's arguments filed 7/24/2003 have been fully considered but they are not persuasive.

In response to applicant's argument that claims 24, 33, 42, 49 recite "a first display driver of the plurality of display drivers to a first and a second memory portion of the plurality of screen memory portions," at page 12, 3rd paragraph. This argument is not persuasive because Zenda '678's invention teaches a first display driver CRT (19) is coupled to a first screen memory portion (5) and a second memory portion "V-RAM (15)", (see figure 8, column 6, lines 16-53).

In response to applicant's argument that claims 24, 33, 42, 49 recite "determine whether the display preferences can be filled in observance of at least one of: configuration properties of the multiple displays and configuration properties of a computing system, the coupling controller determining whether a current configuration of the multiple displays to the computing system can be reconfigured such that the displayed preference can be fulfilled while maintaining effective configuration of the current configuration when the display preferences cannot be fulfilled," at page 13, 2nd paragraph. This argument is not persuasive because Zenda '678 teaches the D-flip flop 59 that controls the gates 55 and 57 (switches 55 and 57) to determine whether the display preferences can be fulfilled in observance of at least one of: configuration properties of the two displays (CRT 19 and PDP 21) and configuration properties of a computing system, the D-flip flop 59 that controls the gates 55 and 57 (switches 55 and 57) for determining whether a current configuration of two displays CRT 19 and PDP 21 to the computing system can be reconfigured such that the display preferences can be fulfilled while maintaining effective configuration of the current configuration when the display preferences cannot be fulfilled (see figure 11A and 11B, column 6, line 61 through column 7, 8, line 14).

For these reasons, the rejections based on Zenda '678 and Zenda '525 have been maintained.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kevin M. Nguyen** whose telephone number is **703-305-6209**. The examiner can normally be reached on MON-THU from 9:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reached on **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Kevin M. Nguyen
Patent Examiner
Art Unit 2674

KN
September 19, 2003

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600